Ukalta Engineering

Product Brief
UGNG-31

3.1 Sigma Uncorrelated Gaussian Noise Generator IP Core

An ultra-compact and fast realization of a digital AWGN

Key Features

- Generates Gaussian distributed samples that match the probability density function of the standard normal distribution within ±1 percent up to ±3.1σ
- Produces uncorrelated Gaussian samples with a flat (white) power spectral density
- Ultra-long repetition period of the output samples
- Efficient on FPGAs, generating 450 million samples/second using a single block memory and fewer than 50 slices *
- Supports multiple uncorrelated instantiations through parameterizable seed values
- Synthesizable for FPGA and ASIC targets using device-independent HDL code

Functional Description

Ukalta's 3.1σ Gaussian noise generator (UGNG-31) produces Gaussian distributed pseudo-random samples with the statistics shown in Table 1.

Table 1: UGNG-31 output sample statistics

Statistic	Value
Mean	0
Variance	1
Spectral flatness	< 0.001 dB
Minimum sample value	-4.8248
Maximum sample value	4.8248
Crest factor	13.6 dB
Repetition period	~10^{34} samples

The UGNG-31 core generates one 16-bit sample every clock period when the clock enable pin is held high. The generated samples are represented in two's complement fixed-point format with a 4-bit integer and 12-bit fraction. Asserting the reset signal clears internal registers of the UGNG-31 and returns the core to its initial state. Figure 1 and Table 2 outline the pin specifications for the UGNG-31 core.

Figure 1: UGNG-31 core block diagram

Table 2: UGNG-31 core pin-out

Pin name	Pin type	Description
CLK	1-bit input	System clock input
CE	1-bit input	Active-high clock enable
RESET	1-bit input	Active-high synchronous reset
n	16-bit output	Gaussian sample output port

The UGNG-31 produces samples that follow the standard normal distribution (i.e. zero mean and unit variance). To obtain a normal distribution with a different mean or variance the user can utilize the UGNG-31 as in Figure 2. The desired variance is obtained by multiplying the UGNG-31 output by the standard deviation of the noise. The mean can be modified by adding the desired mean to the UGNG-31 output.

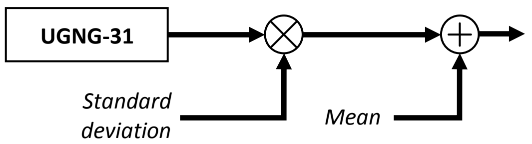

Figure 2: UGNG-31 with programmable variance and mean values

Implementation Performance

The UGNG-31 core is suitable for FPGA devices and ASIC integration. The design does not use multipliers, and on FPGA platforms requires only a single 1024×16-bit block memory and a small fraction of the available logic slices. Implementation results for selected Xilinx and Altera FPGA devices are listed in Table 3.

Table 3: Characteristics of the UGNG-31 core on selected FPGA devices

Device	I	II	III	IV
Clock frequency (*MHz*)	385	470	460	440
Output rate (*MSamp/s*)	385	470	460	440
Slices/Logic modules	105	46	94	94
On-chip memory blocks	1	1	2	2
Dedicated multipliers	0	0	0	0

I: Xilinx Virtex-4 LX 200 -11 (XC4VLX200-11)
II: Xilinx Virtex-5 LX 330 -2 (XC5VLX330-2)
III: Altera Stratix III L340 -C3 (EP3SL340-C3)
IV: Altera Stratix IV GX230 -C3 (EP4SGX230-C3)

Deliverables

- Fully-commented and synthesizable Verilog source code or FPGA netlist
- Bit-true C and Matlab software models
- Instantiation example
- Self-checking test bench
- Product manual and detailed documentation
- Technical support

* only 46 logic slices and one block memory on Virtex-5 devices (see Table 3).

Statistical Accuracy

The probability density function (PDF) for the samples generated by the UGNG-31 core has been calculated using closed-form expressions, yielding an optimized design with precisely defined output statistics. Figure 3 shows the distribution of the generated samples overlaid on the standard normal distribution with linear axes. Figure 4 shows the same plots on a logarithmic y-axis. The generated samples match the theoretical standard normal distribution within ±1 percent relative error up to ±3.1σ. Figure 5 plots the power-spectral density for 5×10^7 generated Gaussian samples and shows excellent spectral flatness.

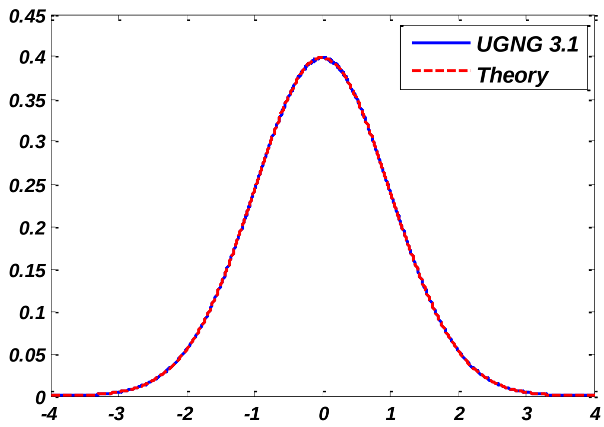

Figure 3: PDF for generated samples and theory

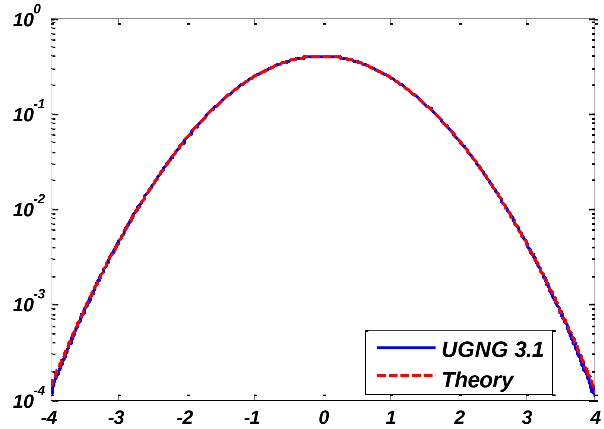

Figure 4: PDF for generated samples and theory on a logarithmic y-axis

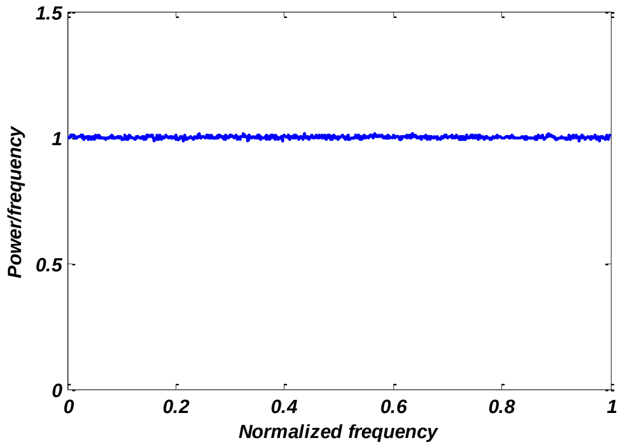

Figure 5: Power spectral density plot for 5×10^7 generated Gaussian samples over 1024 bins

Applications

The UGNG-31 core can be used to model a variety of natural phenomena that exhibit a normal distribution. Gaussian noise generators are widely used as a source of additive white Gaussian noise (AWGN) in communication systems testing. Ukalta's ultra-compact and high-throughput 3.1σ AWGN IP core is suitable for performance measurements of communication systems at high bit error rates (BERs).

Related Products

For validation of systems at lower BERs, an accurate performance evaluation requires a Gaussian noise generator with better tail-accuracy such as Ukalta's 5.7σ and 7.1σ Gaussian noise generator IP cores (see datasheets **UGNG-57** and **UGNG-71**).

The UGNG-31 core can further be used for communications system performance evaluations using more realistic channel models when combined with Ukalta's fading channel simulator IP cores for single and multiple antenna systems.

Ordering Information

For purchasing or to obtain more detailed information on this or any of our other products or services, please contact Ukalta Engineering and we will be pleased to discuss how we can address your special requirements.

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