Product Brief
UMCH-FF-JKS

Basic MIMO Fading Channel Simulator IP Core

Ultra-compact flat-fading channel simulator with Jakes' power spectral density

Key Features

- Generates statistically-accurate Rayleigh and Rician fading samples that are spatially correlated
- Time-correlated samples follow Jakes' isotropic power spectral density
- Supports a variety of MIMO antenna configurations, including 2x2, 2x4, 4x4, and higher order scenarios
- Spatial correlation based on Kronecker, Weichselberger, virtual channel representation and full correlation models.
- Fully-controllable parameters, including the Doppler frequency, Rician *K*-factor, and sample rate
- Easily synthesized for various FPGA implementations using device-independent HDL code
- Ultra-long repetition period of the output fading samples

Functional Description

Each instance of Ukalta's frequency-flat fading channel simulation IP core accurately generates up to eight streams of Rayleigh or Rician fading samples. The samples are time correlated with a power spectral density (PSD) that is given by Jakes' Doppler spectrum. The spatial correlation is based on analytical channel models such as Kronecker, Weichselberger, virtual channel representation (VCR) or full correlation.

Figure 1 demonstrates how a baseband transmitted signal is multiplied by space and time-correlated fading coefficients to generate a received signal impaired by a flat-fading channel. One instance of the UMCH-FF-JKS core generates up to eight complex-valued time-correlated fading samples (i_0,q_0 to i_7,q_7) every clock period when the clock enable (CE) pin is held high. Asserting the reset signal clears internal registers of the UMCH-FF-JKS and returns the core to its initial state. The in-phase components (i_0 to i_7) and quadrature components (q_0 to q_7) are represented in two's complement 16-bit fixed-point format. The matrix processor sub-component applies the MIMO spatial correlation coefficients to the time-correlated samples.

Fading channel simulation parameters such as the spatial correlation coefficients, normalized Doppler frequency, Rician *K*-factor, and angle-of-arrival of the specular component are initialized through a memory interface on the IP core. The configuration values passed on the memory interface are generated with the provided software library. Under manual operation this software library can be accessed through a graphical user interface (GUI) running on a personal computer. Alternatively, the software library can be accessed directly or through a tool command language (TCL) scripting interface and permits for the execution of automated test procedures. Users are able to modify the parameters during the operation of the fading channel simulator using the GUI or the scriptable interface.

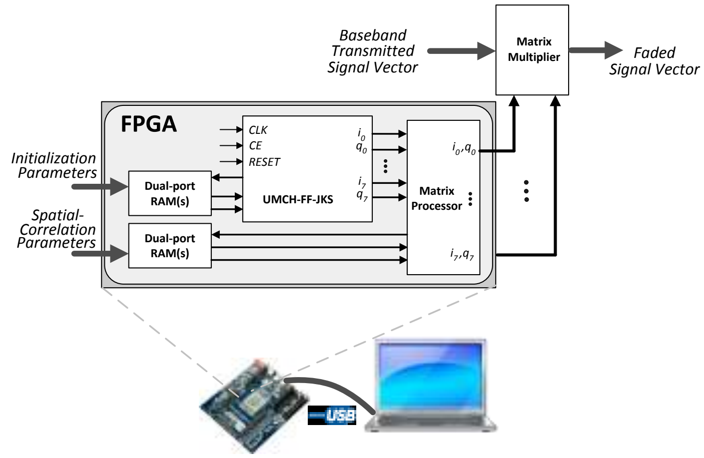

Figure 1: Simulation of flat-fading MIMO channels with Jakes' Doppler spectrum

Implementation Performance

The UMCH-FF-JKS core is ideal for FPGA prototyping of wireless radio propagation channels. The design is coded using device-independent HDL and maps efficiently onto various FPGA architectures. Synthesis results for a 2x2 MIMO fading channel simulator on selected Xilinx and Altera FPGA devices are listed in Table 1. The supported Doppler frequency range is between 73×10^{-6} Hz and 8680 Hz and can be set in steps of 0.001 Hz.

Table 1: Characteristics of the UMCH-FF-JKS core on selected FPGA devices

Device	I	II
Clock frequency (MHz)	257	239
Slices/Logic modules	831 (1.6%)	1545 (1.1%)
On-chip memory blocks	3 (1.0%)	7 (0.7%)
Dedicated multipliers	17 (8.8%)	20 (3.4%)

I: Xilinx Virtex-5 LX 330 -2 (XC5VLX330-2)
II: Altera Stratix III L340 -C3 (EP3SL340-C3)

Applications

MIMO fading channel emulation is a key component in the performance evaluation of emerging MIMO communication systems. The flexibility of the fading IP core allows engineers to rapidly validate and accurately estimate the performance of the baseband algorithms under a variety of radio propagation conditions. It can be utilized to verify the quality of various system components, including source coders, interleavers, modulators, equalizers, channel decoders and detectors. The compact nature of the fading channel simulator enables baseband-level prototyping and debugging of entire communication systems under realistic channel conditions, all on a single FPGA.

Statistical Accuracy

Several statistical measures are applied to the generated fading samples to qualify the output of the fading channel simulator. Time-correlation properties of the generated fading samples are measured using the cross-correlation function (CCF) and auto-correlation function (ACF). Other important aspects of the temporal behaviour of the fading envelope include the level crossing rate (LCR) and the average fade duration (AFD). Figure 2 demonstrates that the generated fading samples match closely with the theoretically predicted statistics. Figure 3 shows the bit-error rates of a prototype 2x2 MIMO system when connected to the fading simulator IP core. Additional statistical data on the fading core output is available upon request.

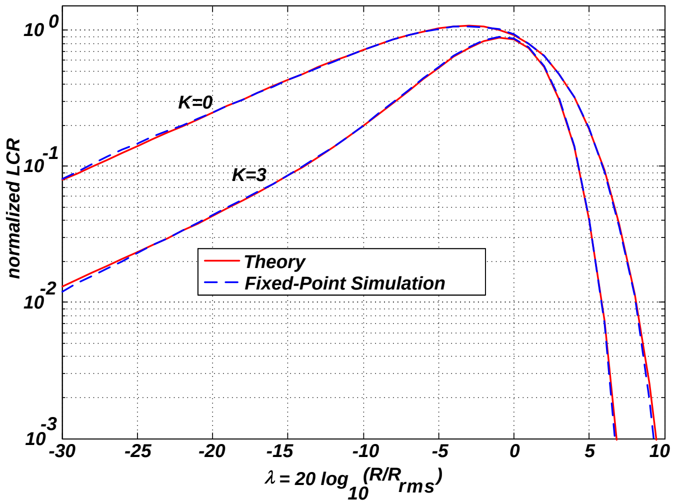

Figure 2: Normalized level crossing rate of the generated fading samples for *K*=0 (Rayleigh) and *K*=3 (Rician) channels

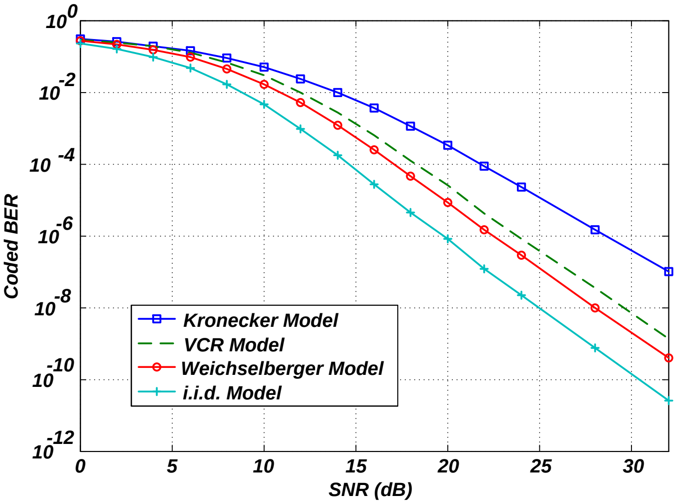

Figure 3: Coded bit-error rate performance of a 2x2 MIMO system with analytical spatial correlation channel models

Deliverables

- Fully-commented and synthesizable Verilog source code or FPGA netlist
- Bit-true C and Matlab software models
- Instantiation example
- Software interface for channel emulator configuration
- Product manual and detailed documentation
- Technical support

Related Products

The fading channel simulator can be combined with Ukalta's noise generator IP cores for the performance verification of wireless communication systems in the presence of Gaussian noise at the receiver. Datasheets **UGNG-31**, **UGNG-57** and **UGNG-71** provide further information on the AWGN IP cores available from Ukalta Engineering.

For emulation of multipath fading channels consider Ukalta's frequency-selective channel simulators from the **UMCH-FS** IP core family. These multipath fading channel simulators provide parameterizable delay values between resolvable paths and can be used to construct arbitrary power-delay profiles (subject to FPGA and off-chip memory constraints).

In case the isotropic Doppler spectrum provided by Jakes' model is not sufficient, Ukalta's **-USD** versions of the fading channel IP cores can simulate arbitrary PSDs including flat, Gaussian, rounded, bell and Jakes' Doppler spectrums. To simulate geometrically modeled channel models please refer to the **-GEO** versions of the fading channel IP cores.

If MIMO fading channel simulation support is not required, Ukalta's **USCH** IP core family provides fading channel simulators for SISO scenarios.

Emulation of fading channels with other distributions such as Nakagami-*m* and Weibull can be performed when combined with Ukalta's **UNAKAGAMI** and **UWEIBULL** IP cores.

Ordering Information

For purchasing or to obtain more detailed information on this or any of our other products or services, please contact Ukalta Engineering and we will be pleased to discuss how we can address your special requirements.

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