

# Basic Fading Channel Simulator IP Core

*Ultra-compact flat-fading channel simulator with Jakes' power spectral density*

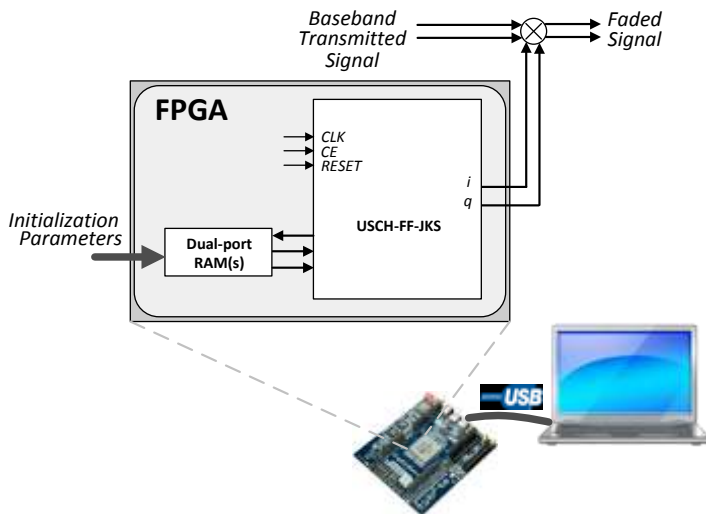
## Key Features

- Generates statistically-accurate Rayleigh and Rician fading samples
- Time-correlated samples follow Jakes' isotropic power spectral density
- Fully-controllable parameters, including the Doppler frequency, Rician  $K$ -factor, and sample rate
- Easily synthesized for various FPGA implementations using device-independent HDL code
- Ultra-long repetition period of the output fading samples

## Functional Description

Ukalta's frequency-flat fading channel simulation IP core accurately generates a stream of Rayleigh or Rician fading samples. The samples are time correlated with a power spectral density (PSD) that is given by Jakes' Doppler spectrum.

Figure 1 demonstrates how a baseband transmitted signal is multiplied by fading coefficients to generate a received signal impaired by a flat-fading channel. The USCH-FF-JKS core generates one complex-valued fading sample ( $i, q$ ) every clock period when the clock enable (CE) pin is held high. Asserting the reset signal clears internal registers of the USCH-FF-JKS and returns the core to its initial state. The in-phase component ( $i$ ) and quadrature component ( $q$ ) are represented in two's complement 16-bit fixed-point format.



**Figure 1: Simulation of flat-fading channels with Jakes' Doppler spectrum**

Fading channel simulation parameters such as the normalized Doppler frequency, Rician  $K$ -factor, and angle-of-arrival of the specular component are initialized through a memory interface on the IP core. The configuration values passed on the memory interface are generated with the provided software library. Under manual operation this software library can be accessed through a graphical user interface (GUI) running on a personal computer. Alternatively, the software library can be accessed directly or through a tool command language (TCL) scripting interface and permits for the execution of automated test procedures. Users are able to modify the parameters during the operation of the fading channel simulator using the GUI or the scriptable interface.

## Implementation Performance

The USCH-FF-JKS core is ideal for FPGA prototyping of wireless radio propagation channels. The design is coded using device-independent HDL and maps efficiently onto various FPGA architectures. Synthesis results for a single-tap fading channel simulator on selected Xilinx and Altera FPGA devices are listed in Table 1. The supported Doppler frequency range is between  $73 \times 10^{-6}$  Hz and 34,700 Hz and can be set in steps of 0.001 Hz.

**Table 1: Characteristics of the USCH-FF-JKS core on selected FPGA devices**

Device	I	II
Clock frequency (MHz)	257	239
Slices/Logic modules	375 (0.7%)	861 (0.6%)
On-chip memory blocks	3 (1.0%)	7 (0.7%)
Dedicated multipliers	6 (3.1%)	9 (1.6%)

I: Xilinx Virtex-5 LX 330 -2 (XC5VLX330-2)

II: Altera Stratix III L340 -C3 (EP3SL340-C3)

## Deliverables

- Fully-commented and synthesizable Verilog source code or FPGA netlist
- Bit-true C and Matlab software models
- Instantiation example
- Software interface for channel emulator configuration
- Product manual and detailed documentation
- Technical support

## Statistical Accuracy

Several statistical measures are applied to the generated fading samples to qualify the output of the fading channel simulator. Time-correlation properties of the generated fading samples are measured using the cross-correlation function (CCF) and auto-correlation function (ACF). Other important aspects of the temporal behaviour of the fading envelope include the level crossing rate (LCR) and the average fade duration (AFD). Figures 2 and 3 demonstrate that the generated fixed-point fading samples match closely with the theoretically predicted statistics. Additional statistical data on the fading core output is available upon request.

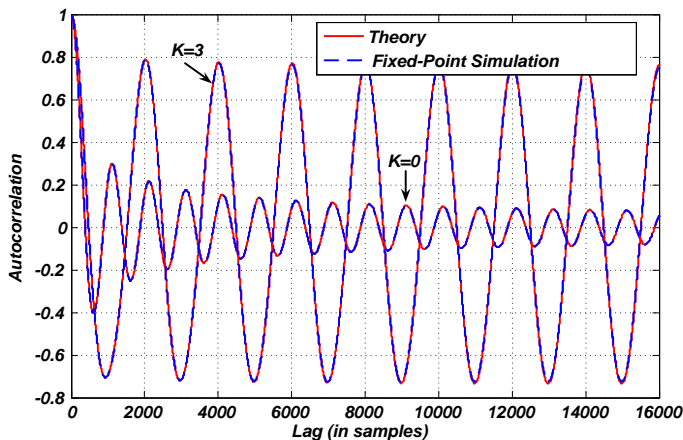


Figure 2: Autocorrelation of the in-phase and quadrature components of the generated fading samples

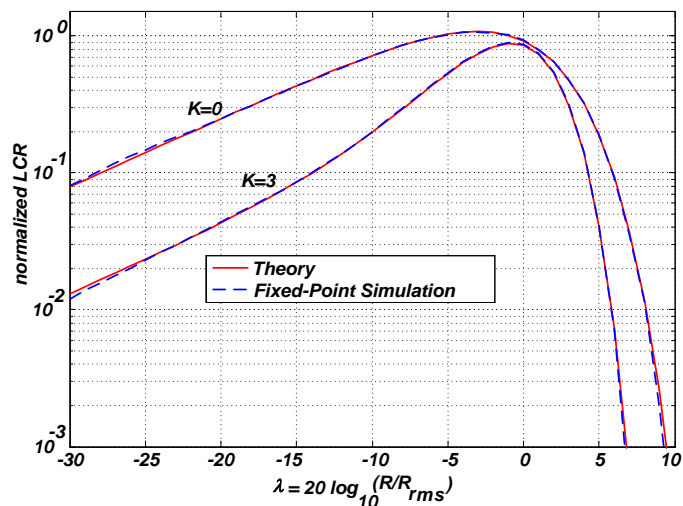


Figure 3: Normalized level crossing rate of the generated fading samples for  $K=0$  (Rayleigh) and  $K=3$  (Rician) channels

## Applications

Fading channel emulation is a key component in the performance evaluation of wireless communication systems. The flexibility of the fading IP core allows engineers to rapidly validate and accurately estimate the performance of the baseband algorithms under a variety of radio propagation conditions. It can be utilized to verify the quality of various system components, including source coders, interleavers, modulators, equalizers, channel decoders and detectors. The compact nature of the fading channel simulator enables baseband-level prototyping and debugging of entire communication systems under realistic channel conditions, all on a single FPGA.

## Related Products

The fading channel simulator can be combined with Ukalta's noise generator IP cores for the performance verification of wireless communication systems in the presence of Gaussian noise at the receiver. Datasheets **UGNG-31**, **UGNG-57** and **UGNG-71** provide further information on the AWGN IP cores available from Ukalta Engineering.

For emulation of multipath fading channels consider Ukalta's frequency-selective channel simulators from the **USCH-FS** IP core family. These multipath fading channel simulators provide parameterizable delay values between resolvable paths and can be used to construct arbitrary power-delay profiles (subject to FPGA and off-chip memory constraints).

In case the isotropic Doppler spectrum provided by Jakes' model is not sufficient, Ukalta's **-USD** versions of the fading channel IP cores can simulate arbitrary PSDs including flat, Gaussian, rounded, bell and Jakes' Doppler spectrums. To simulate geometrically modeled channel models please refer to the **-GEO** versions of the fading channel IP cores.

Multiple antenna (MIMO) fading channel simulation support is available through Ukalta's **UMCH** IP core family.

Emulation of fading channels with other distributions such as Nakagami- $m$  and Weibull can be performed when combined with Ukalta's **UNAKAGAMI** and **UWEIBULL** IP cores.

## Ordering Information

For purchasing or to obtain more detailed information on this or any of our other products or services, please contact Ukalta Engineering and we will be pleased to discuss how we can address your special requirements.

### Ukalta Engineering Corporation

4344 Enterprise Square  
10230 Jasper Avenue NW  
Edmonton, Alberta, T5J 4P6  
Canada

Toll-free: +1 (866) 393 1524  
Phone: +1 (780) 701 1917  
Fax: +1 (866) 380 3755

Email: [contact@ukalta.com](mailto:contact@ukalta.com)  
Web: [www.ukalta.com](http://www.ukalta.com)