

# Multipath Geometric Fading Channel Simulator IP Core

*Ultra-compact geometric frequency-selective fading channel simulator*

## Key Features

- Generates up to eight independently configurable fading paths with parameterizable path delays
- Samples are time-correlated with the Doppler spectrum shape defined by the geometry of the scenario
- Fully-controllable parameters, including the Doppler frequency, Rician  $K$ -factor, and sample rate
- Easily synthesized for various FPGA implementations using device-independent HDL code
- Ultra-long repetition period of the output fading samples

## Functional Description

Each instance of Ukalta’s frequency-selective fading channel simulation IP core accurately generates up to eight streams of Rayleigh or Rician fading samples. The samples are time correlated with a power spectral density (PSD) that is determined by the user-defined scenario geometry.

Figure 1 demonstrates how the baseband transmitted signal is multiplied by fading coefficients to generate a received signal impaired by a multipath fading channel. One instance of the USCH-GEO core generates eight complex-valued fading samples ( $i_0, q_0$  to  $i_7, q_7$ ) every clock period when the clock enable (CE) pin is held high. Asserting the reset signal clears internal registers of the USCH-GEO and returns the core to its initial state. The in-phase components ( $i_0$  to  $i_7$ ) and quadrature components ( $q_0$  to  $q_7$ ) are represented in two’s complement 16-bit fixed-point format.

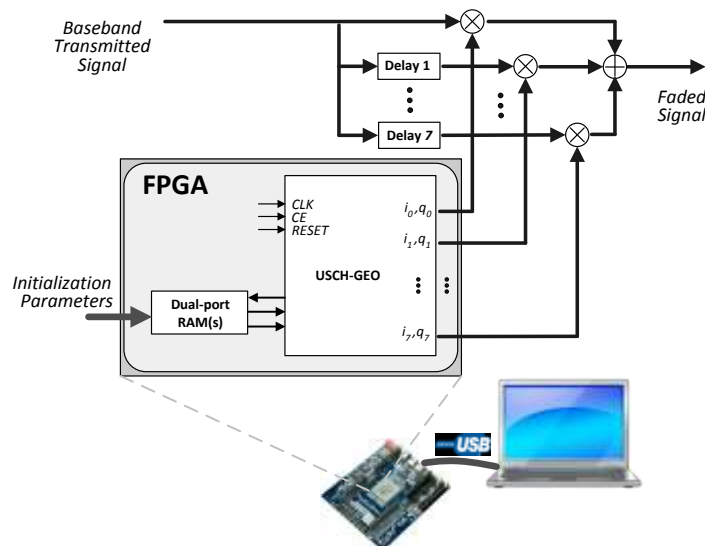


Figure 1: Simulation of multipath geometric fading channels

Fading channel simulation parameters are derived from the geometry of the scenario and path delays and are initialized through a memory interface on the IP core. The configuration values passed on the memory interface are generated with the provided software library. Under manual operation this software library can be accessed through a graphical user interface (GUI) running on a personal computer. Alternatively, the software library can be accessed directly or through a tool command language (TCL) scripting interface and permits for the execution of automated test procedures. Users are able to modify the parameters during the operation of the fading channel simulator using the GUI or the scriptable interface.

The fading channel parameters that depend on the geometry of the scenario are generated by the provided software library. To generate these parameters the user provides the physical constraints of the scenario to the software library, which subsequently calculates the configuration values that can be passed to the IP core’s memory interface. Table 1 provides a listing of the physical constraints that define a geometric channel.

Table 1: Scenario geometry configuration parameters

Parameter	Description
$\zeta$	Distance between transmit and receive antenna
$\omega$	Approximate direction of the direct path from the transmit antenna
$\gamma$	Direction of receiver motion
$Klp$	Rician factor between the transmit and receive antenna
$fD$	Maximum Doppler frequency
$f_i$	Doppler frequency observed from the $i^{th}$ scatterer
$\omega_i$	Direction-of-arrival observed from the $i^{th}$ scatterer
$N_{si}$	Number of independent scatterers for the $i^{th}$ bounce scattering
$q_i$	Amplitude of the received wave from the $i^{th}$ scatterer
$\theta_i$	Phase shift introduced by the $i^{th}$ scatterer
$\xi_i$	Distance of the $i^{th}$ scatterer from the transmit antenna
$\psi_i$	Distance of the $i^{th}$ scatterer from the receive antenna

## Implementation Performance

The USCH-GEO core is ideal for FPGA prototyping of wireless radio propagation channels. The design is coded using device-independent HDL and maps efficiently onto various FPGA architectures. Synthesis results for an eight-tap fading channel simulator on selected Xilinx and Altera FPGA devices are listed in Table 2. The supported Doppler frequency range is between  $73 \times 10^{-6}$  Hz and 4,340 Hz and can be set in steps of 0.001 Hz. For the implementation in Table 2 the maximum path delay is 5.1  $\mu$ s with a delay resolution of 5 ns. The path delay can be increased by allocating additional on-chip memory blocks.

**Table 2: Characteristics of the USCH-GEO core on selected FPGA devices**

Device	I	II
Clock frequency (MHz)	257	239
Slices/Logic modules	1439 (2.8%)	2457 (1.8%)
On-chip memory blocks	17 (5.9%)	35 (3.4%)
Dedicated multipliers	27 (14.1%)	30 (5.2%)

I: Xilinx Virtex-5 LX 330 -2 (XC5VLX330-2)

II: Altera Stratix III L340 -C3 (EP3SL340-C3)

## Statistical Accuracy

Several statistical measures are applied to the generated fading samples to qualify the output of the fading channel simulator. Time-correlation properties of the generated fading samples are measured using the cross-correlation function (CCF) and auto-correlation function (ACF). Other important aspects of the temporal behaviour of the fading envelope include the level crossing rate (LCR) and the average fade duration (AFD). The probability density function (PDF) of the generated samples is compared to the theoretical distribution. Statistical data on the fading core output is available upon request.

## Applications

Fading channel emulation is a key component in the performance evaluation of wireless communication systems. The flexibility of the fading IP core allows engineers to rapidly validate and accurately estimate the performance of the baseband algorithms under a variety of radio propagation conditions. It can be utilized to verify the quality of various system components, including source coders, interleavers, modulators, equalizers, channel decoders and detectors. The compact nature of the fading channel simulator enables baseband-level prototyping and debugging of entire communication systems under realistic channel conditions, all on a single FPGA.

## Deliverables

- Fully-commented and synthesizable Verilog source code or FPGA netlist
- Bit-true C and Matlab software models
- Instantiation example
- Software interface for channel emulator configuration
- Product manual and detailed documentation
- Technical support

## Related Products

The fading channel simulator can be combined with Ukalta's noise generator IP cores for the performance verification of wireless communication systems in the presence of Gaussian noise at the receiver. Datasheets **UGNG-31**, **UGNG-57** and **UGNG-71** provide further information on the AWGN IP cores available from Ukalta Engineering.

If the integer sample period delay resolution offered by this core is not sufficient, Ukalta's **UDLY-FRAC** IP core can be used to generate fractional delays between multipath components.

If stochastic models are required, Ukalta's **-USD** versions of the fading channel IP cores can simulate arbitrary PSDs including flat, Gaussian, rounded, bell and Jakes' Doppler spectrums.

Multiple antenna (MIMO) fading channel simulation support is available through Ukalta's **UMCH** IP core family. The MIMO fading channel simulators support a variety of analytical spatial correlation models including Kronecker, Weichselberger, and virtual channel representation as well as geometrically modeled channels.

Emulation of fading channels with other distributions such as Nakagami-*m* and Weibull can be performed when combined with Ukalta's **UNAKAGAMI** and **UWEIBULL** IP cores.

## Ordering Information

For purchasing or to obtain more detailed information on this or any of our other products or services, please contact Ukalta Engineering and we will be pleased to discuss how we can address your special requirements.

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